

A DETECTOR FOR DETECTING TIMING IN A DATA FLOW

Abstract of the Disclosure

A detector detects timing in a digital data flow with a bit-time equal to T , and with ^{coded mark inversion} (a coding that provides at a beginning of the bit-time no transition, or a transition of a first type, or a transition of a second type, and provides in a middle of the bit-time T no transition, ~~or for the transition of the first type~~). A first circuit generates four local timing signals each having periods substantially equal to the bit-time. Each of the four local timing signals are out of phase with one another by $1/4$ period. A second circuit samples the four local timing signals upon each transition of the first type for determining, based upon the sampling, whether two of the four local timing signals forming a pair of reference signals that are out of phase by $1/2$ period are advanced or delayed relative to the timing of the data flow. The second circuit controls the first circuit for delaying or advancing the four local timing signals based upon the pair of reference signals.